REMARKS

Claims 1-4, 6-10, 12-14, 16-19, 21-23, and 25-32 are pending. Claims 1-4, 6-10, 12-14, 16-19, 21-23, 25 and 26 are allowed.

Applicants Response to Claim Rejections under 35 U.S.C. §103(a)

Claims 27, 28 and 31 are rejected under 35 U.S.C. §103(a) as being unpatenable over **Talwar *et al.*** (U.S. Patent No. 6,380,044) in view of **Guegan** (U.S. Patent No. 5,705,410) further in view of **Esch** (U.S. Patent No. 4,056,825). In response thereto, applicants respectfully traverse on the basis that a *prima facie* case of obviousness has not been established. In order for a claim to be obvious each and every limitation of the claimed invention must be set forth in the cited prior art. In the present instance, there is no teaching in the prior art of the limitation of claim 27 requiring an overlap capacitance between the gate and the source of 0.25(fF/μm/side) or more. The Office Action cites to column 5 and Fig. 5A. of **Esch** for the apparent disclose of "a FET with reduced gate overlap capacitance of source/drain" and "the required gate/source overlap capacitance."

Esch teaches limiting the diffusion area 7' under a metal gate 15' and increasing gate oxide thickness to reduce the parasitic capacitance. The disclosure of column 5 is that the parasitic capacitance of the prior art illustrated in Fig. 5A is 0.034 pf-per-mil along one side of the gate dimension over the diffused region. See col. 5, lines 8-22. This disclosure is contrasted to the invention of **Esch** which is illustrated in Fig. 5B and has a parasitic capacitance of 0.019 pf-per-mil. See col. 5, lines 32-37.

The Office Action appears to maintain that the skilled artizan would derive from this disclosure the motivation to utilize an overlap capacitance, as defined by the current application, of 0.25 (fF/μm/side) or more. Given the above described teachings of **Esch**, applicants respectfully submit that this limitation of claim 27 is not set forth in the reference.

The present invention discloses and claims an index showing the sufficient amount of overlap capacitance in comparison with the conventional amount (0.20(fF/μm/side)). By maintaining the sufficient amount of overlap capacitance, increase in parasitic resistance can be prevented. See page 18 of the specification. Wherefore, applicants respectfully submit that the limitation of claim 27 requiring an overlap capacitance between the gate and source of 0.25 (fF/μm/side) or more is not taught or suggested by the cited prior art.

Claims 29, 30 and 32 are rejected under 35 U.S.C.§103(a) as being unpatenatable over **Talwar *et al.*** (U.S. Patent No. 6,380,044) in view of **Guegan** (U.S. Patent No. 5,705,410) further in view of **Zhang** (U.S. Patent No. 6,855,954). The Office Action specifically points to Figs. 5 and 6 and column 8 of **Zhang**. **Zhang** is directed to a thin film transistor and discloses two insulating films 10 and 11 formed over a gate electrode 4 and separating source 14 and drain 15 regions. Column 8 of **Zhang** discusses that these two insulating layers 10 and 11 have an overlapping parasitic capacitance of 1.04 fF between the gate and source sides. See col. 8, lines 3-29. The Office Action apparently assets that based on this disclosure of **Zhang**, one of skill in the art would be motivated to achieve the claimed overlap capacitance of claim 29.

As with **Esch** above, applicants respectfully submit that this limitation of claim 29 is not set forth in the reference. Specifically, the present invention discloses and claims in claim 29 an index showing the sufficient amount of overlap capacitance, 0.25(fF/μm/side) or more, in comparison with the conventional amount (0.20(fF/μm/side)). By maintaining the sufficient amount of overlap capacitance, increase in parasitic resistance can be prevented. See page 18 of the specification. Wherefore, applicants respectfully submit that the limitation of claim 29 requiring an overlap capacitance between the gate and source of is not taught or suggested by the cited prior art.

In view of the aforementioned amendments and accompanying remarks, Applicants submit that that the claims, as herein amended, are in condition for allowance. Applicants request such action at an early date.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney to arrange for an interview to expedite the disposition of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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